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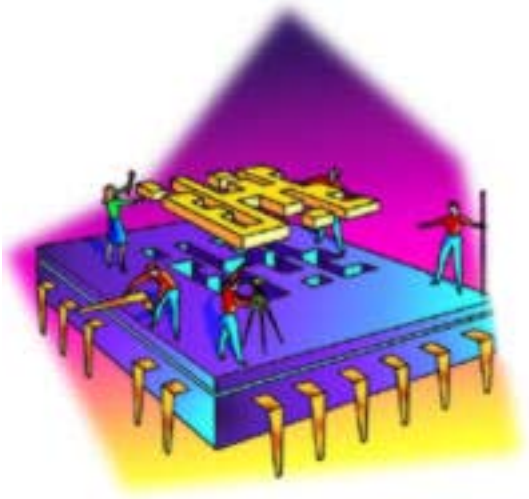
Focused on Semiconductor Innovation and Ventures

Ventures-100

Semiconductor Startup Profiles 2006



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Foreword

Startups are the lifeblood of the semiconductor industry. By following their entrepreneurial instincts, the best and brightest in the chip business are providing focused attention to the innovative ideas critical to advancing IC technology. Some succeed, and some fail; but this process of new ventures budding off from more established firms guarantees a continuous infusion into the industry of fresh ideas and novel approaches. In aggregate, startups represent the cutting edge of semiconductor innovation.

Our primary focus at InsideChips.com is the business of startups. We seek out new companies, find what makes them tick, and profile them in our monthly report, InsideChips.Ventures. Our profiles provide essential information on each startup's history, key executives, financing, strategic focus, business model, technology/ products, competition, strategic partners, and other relevant details.

This volume is comprised of 100 selected startup profiles, arranged alphabetically, that we've published over the last year in InsideChips.Ventures. Some of these companies are in hot new markets, such as wireless sensor networking, while others are attempting to fill the various niches in the emerging area of electronic system level (ESL) design tools. Still others are pushing the envelope with exciting new advances in areas such as software-defined radio and digital power amplifiers.

Ultimately, the Ventures-100 report will provide you with a penetrating look into the current state-of-the-art of semiconductor innovation.

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3Plus1 Technology

3Plus1 Technology is developing a low-power, scalable processor family designed to efficiently run concurrent communications and multimedia applications. The company intends the processor family to enable new kinds of mobile devices, such as multi-functional cell phones, PDAs, cameras and portable PCs with long battery life and flexible, downloadable applications. The company's name refers to "price, power and performance, plus programmability."

The four co-founders are Allan Cox, president and CEO; Amir Zarkesh, executive VP of engineering; Reza Sadri, automation flow architect; and Amit Ramchandran, chief hardware architect. The four men self-funded 3Plus1, and have generated revenue along the way through consulting and authoring several reports. 3Plus1 is now looking for its first round of investment, which it expects to be in the $13 million range.

Prior to co-founding 3Plus1, Cox served one year as COO at Quicksilver Technologies, a venture-backed startup developing adaptive computing machines. He also spent 17 years founding and growing the system LSI business for Toshiba in the Americas. During his career at Toshiba, Cox served as GM for the U.S. enterprise and Sr. VP reporting to the president of Toshiba America. He has also served as CTO for LG Semicon, and began his career at Ferranti Semiconductor.

Zarkesh previously spent three years as director of hardware design for the adaptive computing machine SOC at Quicksilver Technology. For a year prior to this, he founded and was president of Zaias, a data-mining and knowledge engineering software startup. Zarkesh was a co-founder of EDA firm Transcendent Design Technology (acquired by Innoveda, which was bought by Mentor Graphics). He also spent time at the Quad Design group of Viewlogic (acquired by Synopsys).

Sadri is currently the CTO for Procom Technology, where he invented that company's NAS virtualization appliance project and, before that, was chief architect of Procom's NAS product line. Before joining Procom in 1996, Sadri worked for ATT Bell Labs on large database and decision support systems.

Ramchandran is currently responsible for system architecture and logic design in SOC Mosaic at TAEC. Earlier, he was the architect and designer of an adaptive processor for multimedia and communication applications at Quicksilver. He was part of the Intel team that taped out the Pentium-3 M series (Tualatin), and also worked at the Center for Self Organizing and Intelligent Systems (CSOIS Utah), as well as the Space Dynamics Lab and Center of Excellence for Smart Sensors in Utah.

3Plus1 brought in John Hauser to serve as principal software engineer. Hauser was previously a senior DSP engineer at Berkeley Design Technology. Prior to that, he was a programmer in International Computer Science Institute (ICSI), working on ICSI's next-generation vector microprocessor.

These five comprise the company's full-time employees, with 20 others serving part time as consultants. According to 3Plus1, this group of consultants is ready to go full time as soon as the company secures investment funding.

3Plus1's processor family will be targeted at battery-operated digital devices that run multiple applications, such as camera-enabled cell phones, voice-enabled PDAs and wireless cameras. While the manufacturers of these products want to add an increasing number of applications, the typical solutions with the necessary flexibility are a mixture of processors and DSPs — an expensive, time-consuming solution that also has a difficult programming model.

3Plus1 designed its products for a limited set of specific applications, an approach that sets it apart from its competition. The applications are:

- H.263/4-HD, MPEG4
- MP3, AAC, WMP10
- JPEG/JPEG2K
- 2D/3D graphics
- 802.11a/b/g/n/i
- 802.16a/e
- UWB
- Bluetooth
- GPS
- GSM/GPRS/EDGE
- CDMA/CDMA2K/WCDMA/HSDPA

3Plus1's processors run concurrent codecs and basebands; the company calls several applications running concurrently "scenarios." A scenario, for example, could be MP3, H.264, Wimax and JPEG. When the user decides to change functionality, the operating system loads a new scenario from memory; this new scenario could be H.264 and phone (GSM, GPRS and EDGE), which will run until a new scenario is demanded.

3Plus1's inventions are the subject of about 20 patents the company has filed. The fundamental technology, called the CoolProcessor architecture, creates low-power and -area programmable solutions that are very efficient at solving these algorithmic challenges. Secondly, 3Plus1 designed it such that a C compilation and DSP programming model can be used when constructing the total design.

The co-founders spent the first six months of the company's life creating a high-level common database with knowledge of the programming model, hardware and application such that it automatically generates in parallel a set of tools, RTL for the processor, and test vectors. Any

3Plus1 Technology, Cont.

changes made in those areas generate automatic changes to each of the threads. It is somewhat similar to the kinds of things Tensilica has automated, although that company is doing it for a generalized architecture.

3Plus1's family of products is comprised of chips that contain different combinations of its CoolW and CoolN processor cores. The CoolW is very efficient at running wide types of algorithms — 8, 16, 24 and 32 bits – while the CoolN runs 1-, 4-, 8- and 16-bit algorithms.

The first chip 3Plus1 will release is the 3P5220, which is scheduled for launch at the end of 2005. The "5" in the "5220" indicates it has five processors: two CoolWs, two CoolNs, and an ARM926. The second and third numbers in the "5220", both "2", means it has two CoolW and two CoolN processor cores.

The six chips that will comprise 3Plus1's product family range from the 3P3200 (one CoolW, one CoolN and one ARM) for low-end digital devices, to the top-of-the-line 3P9441 (four each of the CoolW and CoolN, plus one ARM), which can run a high-end multi-mode video phone.

In operation, The ARM processor loads a scenario into direct memory access, after which the applications that make up the scenario run completely contained inside the CoolW and CoolN processors. The ARM processor is not used as a controller for those codecs and basebands, and only comes into play again when the user changes the scenario, at which point the ARM drops the first scenario and loads the new one.

3Plus1's processor cores are sub-100 mW, and 120 mw to 400 mW at chip level. The chips are produced in 0.13-micron CMOS at an undisclosed foundry. The company claims the die size is very small, but will not be releasing details until later this year.

Numerous startups are competing in this space, although the majority of them focus on either multimedia or communications; we have not come across another company that is talking about a single architecture that can run multimedia and communications applications for mobile systems. Nonetheless, companies to watch include Stretch, which is developing a software-configurable processor; Sandbridge, the creator of the Sandblaster baseband processor for multi-mode, multi-platform and multi-function wireless terminals and networks; and U.K.-based Icera Semiconductor, a company claiming to have a new class of processor for wireless terminal devices.

(See our profile of Stretch in the June 2004 issue of *InsideChips.Ventures*.; Sandbridge, Dec. 2002; and Icera, July 2003.)

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Date published: March 2005

Achronix Semiconductor

Just over one year old, Achronix Semiconductor is employing asynchronous design technology to create extremely high performance FPGA devices. The company will be offering two product lines, one geared solely toward speed and the other optimized for extreme environments.

Achronix's core technology is the brainchild of Cornell Univ. professor Rajit Manohar, who launched the company with venture capital consultant John Holt in mid-2004. The two founders negotiated an exclusive IP license with Cornell for three patents related to Manohar's work. Achronix is not releasing details of the licensing deal with Cornell, except to say it involves an up-front license, royalties on product sales and a small (less than 10%) equity stake in the company.

Manohar, who serves as CTO, is a pioneer in asynchronous semiconductor technology. He is currently on sabbatical leave as an associate professor of electrical and computer engineering at Cornell, where his group conducts research on all aspects of asynchronous design: circuits, VLSI, system architecture, fault-tolerance, energy efficiency, and design automation. MIT's Technology Review magazine recently selected Manohar as one of the world's "Top Innovators Under 35 in Science and Engineering."

Holt, Achronix's CEO, previously led Saber Security Solutions, a small security technology and venture capital consulting firm in Washington DC. Before that, he was a founding member of the Booz Allen Hamilton Commercial Information Assurance Consulting Practice and served as a founding member of the PricewaterhouseCoopers Commercial Identity Management Security Practice. Earlier, Holt worked in various positions at NASA's Goddard Space Flight Center from 1989 to 1997.

After launching the company, Holt and Manohar brought in two more Cornell researchers, Clinton Kelly and Virantha Ekanayake. Kelly, who serves as VP of advanced research, has led numerous research and product development programs related to ultra-low-power asynchronous microprocessors and FPGAs for the last six years.

Ekanayake, Achronix's VP of engineering, recently joined Johns Hopkins Univ. as an assistant professor in the Department of Electrical and Computer Engineering, where his research group focuses on asynchronous VLSI and architecture. Outside of academia, his experience includes stints at Netscape Communications, Telcordia (formerly Bell Communications Research), and, most recently, Intel.

Manohar and Holt have thus far self-funded Achronix, contributing a little over $1 million of their own capital. Achronix, whose four executives comprise the company's entire staff, is fairly confident it can get to product shipping in Q4 2006 with its current cash resources, but expects to seek funding to scale up operations after that.

Fulcrum Microsystems is probably the best-known and -funded asynchronous design company. Although Achronix and Fulcrum are targeting different areas, Achronix hopes to succeed by taking a similar approach as Fulcrum: employing an asynchronous core for the high-speed processing, but surrounding it with synchronous interfaces so the device can drop into any existing system.

Achronix has put significant effort into the software side to enable the use of existing EDA tools, so that customers can use their traditional VHDL/Verilog descriptions and not need to know anything about how asynchronous design works. This is a different philosophy from that of past asynchronous companies, which often set out to change the way circuits are designed.

Achronix is both shipping internally developed tools and partnering with other EDA vendors to support the products.

Achronix is initially developing two product lines, ULTRA and XTREME. The ULTRA line of FPGAs is designed for pure speed, operating at over 1GHz. The somewhat slower XTREME line of FPGAs is designed to operate in high radiation and extreme temperature environments.

The company will release the high-performance ULTRA line of FPGAs first. The prototype of this device, built in 0.18-micron CMOS, has an initial total system throughput performance – as opposed to maximum internal clock speed — of 674 MHz. Throughput varies dramatically depending on the design, but Achronix claims that while typical designs with Altera or Xilinx FPGAs can achieve 20% to 80% of maximum internal clock speed, its asynchronous devices put users in the 50% to 80% utilization range of the maximum.

While the ULTRA prototype employed 0.18-micron technology, the production versions will be built in 90-nm technology. At 90 nm, Achronix expects to at least double the performance. The first product in the Achronix-ULTRA line will be released in Q2 2006 and will operate at speeds over 1 GHz.

Based on ULTRA, the XTREME line will be modified to provide greater radiation tolerance. Achronix, which expects to release XTREME in 2007, will market the line as a lower density extreme environment product. The volumes in the market are quite low, but the margins are excellent.

After launching these first two product lines, Achronix believes it will be able to produce prototype devices in the 2- to 3-GHz range by late 2007, and ship them in 2008.

Achronix does not intend to capture market share from a specific Xilinx or Altera part, but is instead targeting an extremely high-performance niche in the market. Achronix is not trying to be all things to all people, offering slight improvements of speed, power and density. The company

Achronix Semiconductor, Cont.

is instead focusing primarily on speed, which is the company's core strength.

Achronix intends to achieve densities that are either equivalent or slightly lower than current Virtex-4 or Stratix II type devices. Asynchronous circuits are inherently more power efficient than synchronous circuits, so the company believes it is competitive in terms of power. But it is the extremely high throughput that is the company's key market differentiator. Because Achronix will be able to offer 1-GHz throughput, the company maintains that having slightly lower density than high-end Xilinx or Altera chips will not be a showstopper for most potential customers.

In addition to the traditional FPGA market, Achronix believes it can also capture part of the market that's dominated by ASICs. This is the area the company is actually most excited about in the long term.

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Date published:November 2005

Aegis Semiconductor

Princeton University spin-off Aegis Semiconductor is combining optical interference coatings and thin-film semiconductor materials to create dynamically tunable optical products. Tunable components have historically been an expensive, premium product that manufacturers built into their equipment as little as possible. Aegis developed its Active Thin Films technology platform to enable mass applications by offering tunable filters for hundreds of dollars instead of the usual thousands.

Matthias Wagner launched Aegis in Jan. 2000 with a small group of PhD graduate students from the Princeton University Center for Photonics and Optoelectronic. The founding idea was to employ flat-panel display industry technology, specifically thin-film amorphous semiconductors, in optical communications devices.

Wagner, who heads the company as CEO, previously served as COO/CFO of Knite, an engine electronics company. He has also worked with Princeton Consultants, and he began his career as a production engineer with Panasonic in Osaka, Japan. Wagner was recently named a finalist for Ernst & Young's New England Entrepreneur of the Year Award.

Aegis has raised $27 million over three rounds of funding. YankeeTek and Stata provided an initial $1 million in summer 2000, and both companies participated in the following two rounds as well. Vesbridge Partners led both the Nov. 2001 $16 million round and the May 2004 $10 million round.

The company set up headquarters in Woburn, Mass., and employs about 40 people. Aegis' expertise is in wafer fabrication, and thus maintains its own modest 1,500-sqaure-foot fab. To keep costs low, all packaging and assembly are performed in Asia.

Telecommunications companies have been developing tunable filters for the past five years, but Aegis intends to trump them with a much more cost-effective platform. While the majority of companies developing tunable components employ a MEMS-based approach, Aegis is pioneering a solid state, silicon-based approach, which is not only highly reliable, says Aegis, but also 10-times lower in cost than the MEMS devices.

Aegis' tunable filter employs a multi-layered interference structure, a well-known design in which one narrow range of colors is transmitted while the rest are reflected. Aegis makes the structure tunable by integrating a resistive heating layer with thin-film semiconductor materials that have temperature-dependent properties. The temperature of the semiconductor layer determines which wavelength of light will be transmitted through the filter, and adjusting the heating layer changes the transmitted wavelength (see Figure 1).

Aegis' technology is markedly different from the predominant available tunable technology, which employs a similar filter structure but controls the wavelength by mechanically separating layers of the filter. With their moving parts, these tend to be complex, expensive devices.

Packaging is another important part of Aegis' story. To keep costs low, the company uses an inexpensive detector package, which is typically used for low-cost receivers. Aegis modifies the detector package to include the tunable filter, resulting in a simple stack-up assembly that can be performed inexpensively in East Asia, and which provides a very high yield.

Aegis performs wafer coating and patterning in-house, as well as wafer-level testing on its modified semiconductor prober. The company also does the dicing and sorting in Woburn, but may soon outsource those tasks to its contractor in Thailand, which currently does all the assembly, burn-in, component test and pig-tailing.

Aegis is slowly moving toward greater levels of outside contracting, and is actually outsourcing everything but the coating step for its next product line. The company may eventually employ a model where a MEMS foundry could either obtain an appropriate coating capacity, or Aegis could install it at the foundry.

Aegis' first two products lines are channel-monitoring devices and tunable filters. The demand for tunable filters is just starting to pick up, but there is already demand for channel monitors. Cable companies, for example, are eager for the ability to remotely monitor traffic at a particular node and make needed adjustments remotely, rather than dispatching a technician out to the node.

The channel-monitoring line is comprised of the mosquito® tunable optical detector (TOD), as well as two module-level products: the channel tilt monitor (mosquito® CTM) and optical channel monitor (mosquito® OCM).

The price ranges for Aegis' channel-monitoring line, which began shipping this year, are volume dependent, but in large volumes the rough price for the mosquito tunable detector is $600 to $800 per unit. The module-level channel tilt monitor in small quantities is in the $1,500 range, and the more fully featured monitoring products are in the $1,800 range.

The next step for companies that maintain telecommunications equipment is to be able to reconfigure the network by turning on capacity as it's required, and that's where Aegis' tunable filter components come in. The ASE tunable filter, called the hornet™ TOF A1, is intended for noise filtering in a single-channel system. Demand for this kind of product comes primarily from China, which is experiencing a good deal of single-channel system build-out. Aegis is also developing the hornet™ TOF 100 DWDM tunable filter. These parts are sampling now and will be available sometime in the second half of 2005.

Aegis is also looking at non-telecom applications that

Aegis Semiconductor, Cont.

could benefit from tunable components. The company is conducting preliminary work with customers in areas such as spectroscopy and thermal imaging.

Aegis has two announced customers thus far. The first, Avanex, is including the company's optical channel monitoring module in its PowerWatcher rack-level monitoring system. The other, Israel-based RED-C Optical Networks, is integrating the component-level tunable optical detector into its Senitor self-managed optical amplifiers.

The largest equipment vendors and potential customers in this industry include Nortel Networks, Lucent Technologies, Alcatel, Hitachi, Fujitsu and Siemens. Many of these established companies used to have vertically integrated operations, building components they would integrate all the way up to the system level. One of the big changes in the industry over the last five years is that these systems companies no longer insist on producing their own optical components. They are focusing their resources on system-level design and software, and are increasingly even buying complete optical subsystems. This is less true in Japan and China, but in general the telecom industry is much more hospitable to buying from third-party vendors such as Aegis.

Aegis' management team also includes CTO Eugene Ma, who previously spent several years as a consultant in the Advanced Technology Group at Andersen Consulting. At Princeton, he developed advanced thin-film semiconductor devices and processes for low-cost, flexible flat-panel displays, and has authored multiple patents pending in the area of active thin film devices.

Lawrence Domash, chief scientist, served as division manager of the Photonics Group at Foster-Miller. Earlier, Domash developed novel optical fiber sensors, photo-refractive devices, and new methods of diffractive micro-optics. He has three issued U.S. patents, with others pending.

Wayne Sharfin serves as VP of engineering. Prior to Aegis, Sharfin was VP of engineering at Telephotonics, and held several key management positions at Lasertron (acquired by Corning). He also held optoelectronics research positions at GTE Laboratories and MIT's Lincoln Lab.

Gary Ainsworth, VP of operations, joined Aegis from Maxtor, where he was responsible for test development. Previously, he was a commercialization consultant, and also served as director of manufacturing for Lasertron's Pump Division.

Lyle Chalupsky, VP of sales and marketing, spent 21 years at ADC Telecommunications, where his most recent position was VP of global sales for ADC's Connectivity, Systems Integration Services and Access Products lines. He also held various sales, management, marketing and customer service positions.

David Parent is the company's VP of finance and administration. Parent previously served as director of finance and controller for Integral Access, a supplier of IP-based access equipment. Prior to that, he held numerous accounting and finance positions at National Semiconductor and Wright Express.

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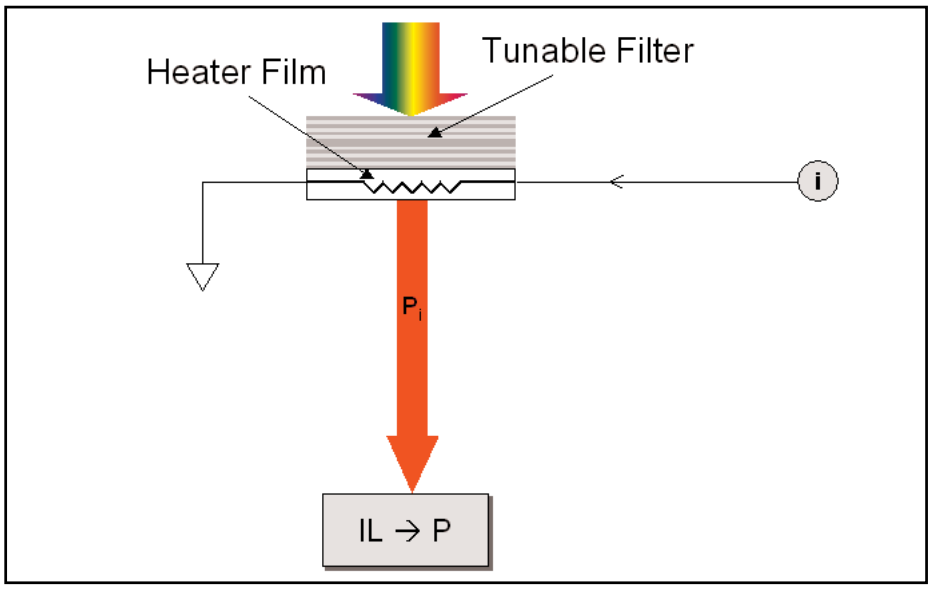
Date published: Dec. 2004

Figure 1 -- Aegis' Tunable Filter



AGEIA Technologies

Since emerging from stealth mode in mid-2005, AGEIA Technologies has created quite a buzz among computer gaming aficionados, who eagerly await the company's PhysX processor. PhysX is a physics processor, specifically designed to take static game-based settings to the next level of responsive, unscripted physical reality. PhysX handles the physics processing required anytime two objects collide and their trajectories change, for example, or when a tank explodes and the resulting thousands of flying objects must interact with each other.

The letters in the name "AGEIA" stand for the five founders' countries of origin – Germany, Egypt, India and two from America.

Manju Hegde, CEO and chairman, is a professor of electrical engineering at Washington Univ. in St. Louis, Mo. His professional experience includes 15 years of research and consulting for companies such as Southwestern Bell, Bellcore, Eatel and Teleware. He is one of the founders of Celox Networks, and served as its CTO. Prior to that he was chief scientist at MinMax Technologies.

Curtis Davis, president and COO, was the initial CEO and subsequently the VP of engineering at Celox Networks. Before that, he was the director of business development at MinMax Technologies and, ealier, lead project engineer for MEMC.

Otto Schmid, VP of hardware engineering, is one of the founders of Celox Networks, where he served as chief hardware architect, director of VLSI, and AVP of hardware. Prior to Celox, Schmid was an engineering manager at MinMax Technologies.

Jean Bordes, AGEIA's senior architect, worked extensively in the field of computer graphics at the Rensselaer Design Research Center. He is one of the founders of Celox Networks, where he served as chief software architect, and was responsible for all software development at MinMax Technologies. Earlier, he was network software engineer for Meridian Technology.

Monier Maher, senior architect, was a co-founder of Celox Networks and served as its chief system engineer. Prior to that, he was a design engineer at Minmax Technologies.

The co-founders launched AGEIA in 2002, and have raised approximately $58 million over three rounds of funding from Apex Venture Partners, HIG Ventures, Granite Global, BA Venture Partners, VentureTech Alliance, and CID Ventures.

The company is not disclosing the number of employees so as not to provide potential competitors with a clue to the development resources necessary to create a physics processor. AGEIA has offices in Sweden, Switzerland, China, India and the U.S. (St. Louis and Mountain View, Calif.).

Most games today already use physics, which is performed in the CPU in PCs. But general purpose CPUs are not designed to be simulation processors, and cannot provide physics processing at a high level. While they might be able to handle, for example, 20 flying objects from an explosion, 20,000 objects would be out of the question.

The PhysX processor offloads software physics processing from the CPU and graphics processor (GPU). In terms of function, the CPU will continue to orchestrate, the GPU will render and display, and PhysX will control the movement and interaction aspects within the game.

PhysX accelerates everything from physical object interactions to fluid-based particle effects such as water and smoke. Initial features already incorporated into the product are:

• Rigid body dynamics – Massive explosions and debris.

• Fluid dynamics — Wall of lava, for example, and water that behaves like water, not just looks like it.

AGEIA will be bringing out additional features as driver updates over the next year:

• Soft body dynamics — Gelatinous creatures.

• Hair simulation — Windswept hair.

• Clothing simulation — Loose flowing clothes.

• Finite element analysis — Crumpling fenders.

• Universal collision detection — Fully reactive surroundings.

AGEIA offers PhysX technology in two versions, the actual processor and a software-development kit. The PhysX processor, built in TSMC's 0.13-micron process, is a 20-watt, 125-million-transistor device and is 182 square millimeters. AGEIA is marketing the processor on a PCI card, for which the company has inked deals with board manufacturers ASUS and BFG Technologies.

While a separate board product means gamers will have to buy a physics board in addition to a graphics board, AGEIA opted to go this route instead of integrating PhysX onto a graphics board for several reasons. On the technical side, even if PhysX is sitting right next to the GPU it will still communicate with the graphics chip through the CPU, so integrating them on the same board provides no added value. Secondly, the boards need cooling and they are both already hot. And perhaps the most important reason, according to AGEIA, is that gamers do not like to be told which graphics board they must use.

The SDK, which has been available for the last 18 months, enables game developers to implement game features that will leverage the hardware acceleration of the PhysX chip, and also supports next-generation game platforms Xbox 360 and Sony PlayStation 3.

AGEIA Technologies, Cont.

Although AGEIA's market focus is the PC space, the strategy behind supporting the Microsoft and Sony console platforms is to maximize the amount of content available to run on its processor. Rather than develop games for a single platform, game developers want to address Xbox, PlayStation and PCs with the same game. If game developers employ PhysX software to create their console-based games, the PC version of those games will necessarily have equal or better physics capabilities.

Under a strategic licensing agreement reached in July, Sony will bundle AGEIA's SDK along with the PlayStation 3 development kits.

AGEIA is releasing the PhysX processor in Q4 2005. The PhysX-powered boards manufactured by ASUS and BFG will likely have consumer pricing in the $249 to $299 range.

AGEIA has a number of content-side customers that support PhysX, including EPIC, which is now the dominant PC game engine (EPIC both uses its Unreal 3 engine for its own games and licenses it to other game developers). Other key customers for AGEIA include Ubisoft, Icarus Studios, Cryptic Studios, Phantagram, Digital Jesters and others.

AGEIA has made two acquisitions along the way, Meqon Research in Sept. 2005 and Novodex in early 2004. Meqon, a physics development company based in Sweden, developed a well-received physics solution called the Meqon Game Dynamics SDK, which AGEIA incorporated into the PhysX SDK. Novodex is an ETH Zurich spin-off whose software became the basis for the PhysX SDK.

The physics processor is a unique product, and we are not aware of any competitors building a similar device. In the near future, the most likely physics-acceleration competition to emerge will likely be in the form of software, which will not be a significant threat to a dedicated processor.

One source of potential competition on the hardware side could be those companies already in the gaming industry, most notably nVIDIA and ATI Semiconductor. AGEIA has been collaborating with both of these companies on demos, as PhysX shows off very nicely these companies' graphics technologies. So at least in the near term, AGEIA appears to be complementary to nVIDIA and ATI. Whether the two graphics giants have their own plans for physics acceleration devices remains to be seen.

The management team includes Rafael Solari as VP of finance. Most recently, Solari led the financial operation at Velio Communications (which sold its IP licensing business to Rambus and its chip business to LSI Logic). He has also held financial management roles at Intel, Cirrus Logic and MMC Networks.

Greg Stoner, VP of business development, previously worked at Metrowerks, a Freescale Company, where he was the CTO and GM of the Console Games Business. Prior to Metrowerks, Stoner was with MIPS Technology as the manager of application engineering and marketing.

Kathy Schoback is AGEIA's VP of content acquisition. Schoback held a variety of relationship-management and business-development positions during nine years at Sega, including director of external development and publishing. She also served as director of product operations at Eidos.

Sanjay Patel, chief architect, is currently a professor in the Electrical and Computer Engineering Department at the Univ. of Illinois/Urbana-Champaign. Patel has gained industrial experience at companies such as Digital Equipment Corporation, Intel and HAL Computer Systems, and consults extensively for high-tech organizations such as Transmeta, Jet Propulsion Laboratory, HAL, and Intel.

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Date published:November 2005

aJile Systems

AJile Systems is a six-year-old company pioneering Java-based processors. Founded in July 1999, aJile is offering a family of low-power networked single-chip Java microprocessors and IP cores to extend the Java paradigm beyond the desktop and server to a wide variety of handheld, mobile and consumer appliances.

The seven founders are veterans of Rockwell Collins, Sun Microsystems, and Centaur Technologies. This group includes four of the principal engineers and designers that developed the world's first low-power Java processor, the Java Embedded Microprocessor (JEM™), as well as advanced Java software development tools at Rockwell Collins.

The JEM1 direct execution Java microprocessor achieved its first silicon in 1997. JEM technology enables low-power embedded applications to be programmed entirely and directly in Java, while also enabling them to achieve the efficiency and performance of comparable conventional embedded processors programmed in C.

aJile's solutions are based on JEM technology, for which the startup has an exclusive license with Rockwell.

CEO George Hwang began his career in 1969 at National Semiconductor as a TTL design engineer, then joined the IC technology development group at Hewlett Packard. In 1980, Hwang led a team from Hewlett-Packard to start his first company, Integrated Device Technology (IDT), which went public in 1984. He launched his second company, ULSI Systems, in 1987.

CTO David Hardin is a well-known expert in the fields of real-time Java and formal methods. Hardin is a primary member of Sun's Real-Time Java Expert Group, and has been involved with real-time embedded Java requirements development since it began with the National Institute for Standards and Technology in June of 1998.

Danh Le Ngoc, who serves as VP of sales and marketing, has more than 23 years of semiconductor experience in product marketing, product definition and applications engineering. He has developed Java processor products, embedded DRAM based 2D/3D graphics accelerators, the embedded RISC MIPS processor, DSPs, bit slice machines, and numerous others. He served as group marketing manager for PicoJava at SUN.

Nick Mykris is aJile's VP of engineering. While at Rockwell Collins, Mykris was a technical manager in the Advanced Technology Center responsible for the development of proprietary stack processors and support environments, including the JEM microprocessor.

Allen Mass, senior engineer, is an embedded systems designer with more than 20 years of experience in HW/SW design, integration, and debug.

Mike Masters, chief hardware architect, has developed CPUs used in embedded systems that vary from highly reliable autopilot applications to low-power GPS engines. He led Rockwell Collins' JEM1 processor design activity that resulted in the world's first Java microprocessor in 1997.

B. Ramkumar, the company's chief software architect, served on the research faculty in Electrical and Computer Engineering at the University of Illinois-Urbana for nearly two years, and then in the Electrical and Computer Engineering department at the University of Iowa for five years, prior to founding Centaur Technologies in 1997.

aJile has raised approximately $10 million thus far. The company's backers include a small venture capital firm, Synapse Capital, as well as several small, un-named companies and numerous angel investors.

aJile is banking on a significant shift occurring from the "desktop-centric" computing model to a "network-centric" model, which is accelerating the need for new generations of 32-bit low-power Java processors. These new embedded Java processors must effectively and securely execute distributed objects over wired and wireless networks.

Under the JEM licensing agreement with Rockwell, aJile has exclusive rights to commercialize existing JEM technologies, as well as to further develop new extensions of the core JEM architecture and technology.

The company's aJ-100 distributed SOC represents the second generation of the JEM™ processors developed at Rockwell Collins. One of the unique implementations of aJile's platform is a multiple JVM feature, which enables multiple Java virtual machines to coexist in the hardware. Each of the JVMs can have its own kernel, thread manager, and resources such as I/O and memory, allowing multiple independent Java applications to execute in a deterministic, time-sliced schedule with full memory protection. For example, one JVM could be dedicated to the private environment, such as a home network, while a second JVM is dedicated to the broadband network. This feature represents one of the key patents aJile has filed.

aJile's aJ-100 also allocates a portion of the on-board SRAM for custom instruction microcode. For example, a customer may want to add a new instruction set to the platform to enhance performance of graphics, security, or any number of things.

Other features include:

- Fast real-time performance of less than 1msec latency, which means the technology could even be used at the sensor level.
- Low power consumption of less than 1mW/Mhz.
- Networking capability of TCP/IP.
- Enhanced security.

aJile Systems, Cont.

Two other startups to watch in this space are Velocity Semiconductor and Nazomi Communications. While aJile provides a pure Java processor, Velocity's micro-controllers support mixed-language development employing industry-standard legacy C code and Java. Nazomi, a supplier of Java hardware acceleration technology, has already made significant inroads into the cell phone market, with more than three million phones incorporating its technology.

(See our profile of Velocity in the Aug. 2003 issue of *InsideChips.Ventures*, and Nazomi in the Nov. 2003 issue.)

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Date published: March 2005

Ambric

Ambric, a startup still in stealth mode, is developing a new programmable chip platform.

Jay Eisenlohr, who serves as president and CEO, and Anthony Mark Jones, VP of engineering and CTO, founded the company in Jan. 2003. Eisenlohr has spent more than 25 years in the semiconductor and EDA industries. Ambric is the third startup he has founded. Micron Technology acquired his most recent company, Rendition, for $125 million. His sold his first startup, Aris, to Apple. Jones, who holds 48 patents, has spent 23 years in the IC industry, has deep expertise in all aspects of analog, digital, and system IC design. The two met at Rendition.

Ambrid's chairman is Steve Sharp, who formerly served as president and CEO of TriQuint Semiconductor, and presently is a TriQuint board member.

In Sept. 2004, the company completed its $10.4 million Series A financing. ComVentures and OVP Venture Partners co-led the round, which included all of Ambric's seed-stage investors, including Northwest Technology Ventures and private investors.

Ambric, which employs 19 people, is developing a reconfigurable architecture that the company says is quite different from a traditional reconfigurable processor. At this point, the company is not revealing any details about its products.

Reconfigurable processor technology has attracted a great deal of interest, and the field has become quite crowded. Competitors include NEC, Tensilica, Analog Devices, Intel and Philips, as well as a bevy of startups. Improv, for example, developed a configurable multiprocessor architecture, called Jazz; PACT XPP Technologies has a coprocessor that is reconfigurable on-the-fly, enabling a "virtual ASIC"; Elixent, a spin-out of a new reconfigurable algorithm processor (RAP) technology from Hewlett-Packard's printer business unit, developed a RAP platform that implements algorithms in "virtual hardware," enabling the creation of a hardware accelerator for every algorithm in a system; and Leopard Logic enables customers to move embedded FPGA onto a system-level ASIC. Other competitors in this space include Silicon Hive, picoChip Designs, QuickSilver Technology, Infineon (through its acquisition of Morphics Technology), IPFlex, ON DEMAND Microelectronics, Mathstar and Stretch.

For more information on competing technologies, see our profiles of QuickSilver in the May 2002 issue of InsideChips.Ventures; PACT, Aug. 2002; Improv Systems, Sept. 2002; Leopard Logic, Sept. 2002; Elixent, May 2003; IPFlex, Nov. 2002; picoChip, Aug. 2002; Stretch, June 2004; ON DEMAND, Aug. 2004; and Mathstar, Oct. 2004.

We will revisit Ambric with an updated profile as soon as the company is ready to divulge more information about its products and technology.

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Date published:November 2004

Amulet Technologies

Two colleagues with backgrounds in electronic automotive diagnostic equipment, Willy Borner and Ken Klask, founded Amulet Technologies to develop graphical user interface (GUI) systems for electronic devices. Launched in Sept. 1998, Amulet provides chips, modules and board-level solutions that enable customers to easily create high-quality user interfaces with a minimum of development effort.

Klask and Borner were previously with Snap-On Tools, a company best known for its hardware tools that began offering instrumentation products in an effort to position itself as an end-to-end solution for technicians. The two arrived at Snap-On via its acquisition of Balco, a company founded by Borner that developed electronic automotive diagnostic equipment. While at Snap-On, Borner and Klask went looking for a bolt-on GUI to provide a mid-life kicker for certain Snap-On products. After discovering that the solution did not exist, they founded Amulet to fill that niche.

Borner, who serves as the director of business development, co-founded Balco in 1979. Balco, which became a division of Snap-On in 1991, was active worldwide and grew to $50 million in sales in 1997. Borner continued to manage the division until 1996. He was also a co-founder of Nortron, a manufacturer of automotive service equipment founded in Australia in 1971 and California in 1974.

Klask is Amulet's president and the architect of the company's IP. Klask previously worked at Balco/Snap-On for 11 years, most recently managing the development of firmware for all of Balco's handheld instrumentation products as manager of electronics design. As an electronics design engineer, Klask designed the digital ASIC and analog interface circuitry used in all of Snap-On's vehicle communications cartridges. Prior to Balco, he designed microprocessor-based data-acquisition and -control systems at Westinghouse Electric, developed flight control firmware at NASA's Ames Research Center, and briefly taught microprocessor interfacing at San Jose State Univ.

As director of sales and marketing, Jim Todd is the company's spokesman and technology evangelist. Todd was most recently employed at Future Electronics as sales account manager working in semiconductor sales, lead development and design demand creation for silicon suppliers. Previously, he was the director of sales and marketing at Snap-on Diagnostics, a division of Snap-on Tools.

The 10-person company initially bootstrapped itself, and then raised a bit less than $5 million over two rounds of funding from angel investors. In the mid-2005 timeframe, Amulet expects to begin looking for strategic partners and venture capital.

Just as in Microsoft Windows, the processor in embedded products typically spends about 50% or more of its time driving what is seen in the GUI. Amulet's solution provides a dedicated microcontroller to do all the heavy lifting for the user interface, relieving the host processor from that burden. As a consequence, customers can choose a lower-power host processor that only needs to drive the actual application.

Amulet has essentially developed a graphical operating system on a chip containing a microprocessor, LCD controller, and graphics library. By employing HTML authoring tools, the company enables non-programmers such as graphic artists and usability specialists to create good-looking content in a manner similar to web pages. The benefit to customers is that they can create a more robust and intuitive GUI in hours or days, as opposed to weeks or months using traditional software methods.

Amulet is targeting companies that develop embedded systems products and portable or mobile digital devices that employ GUIs to convey information and interact with human operators. Potential customers are OEMs in a wide variety of markets, including building security, home controls, law enforcement, point-of-sale machines, and fitness, office, audio and manufacturing equipment.

The company supports just about all the monochrome graphics displays on the market, with the exception of displays beyond VGA on the upper end, and cell phone displays on the lower end. Amulet has thus far focused on industrial markets, although it will soon be expanding into cell phones and other consumer electronics.

Amulet's products include 5.7- and 3.8-inch controller boards and fully integrated modules, as well as the chips. The controller boards include the graphical OS chip, memory, touch screen decoder, backlight and LCD bias supplies, and serial interface. The boards support single-scan monochrome displays up to full-VGA resolution.

The modules, which currently represent most of Amulet's business, are displays with the controller built in. These enable customers to concentrate on their applications, and then easily drop in a 5.7- or 3.8-inch GUI.

Amulet has picked up a number of customers, including LOUD Technologies, which has incorporated Amulet's technology into its Mackie brand of recording equipment, and an un-named customer that is designing Amulet into point-of-sale equipment going into all of Arco's gas stations. Stoelting, a manufacturer of lab equipment, is also a major customer.

In addition, Intel's reference design for its Sandow entertainment PC includes Amulet in the front panel.

Ultimately, Amulet has identified a need for GUI technology specifically designed for mid-range applications, which are not well served by existing methods of creating user interfaces. The always-increasing number of devices requiring GUIs spans a huge range of markets and industries,

Amulet Technologies, Cont.

providing the company with significant growth opportunities. We believe one of Amulet's greatest initial draws is its ability to enable customers to provide a mid-life remodel to their products by adding a GUI while retaining their legacy hardware and code. We expect Amulet will also be successful in the consumer electronics market, once it makes its push into that arena.

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Date Published: December 2004